OSTROLENK, FABER, GERB & SOFFEN, LLP
Attorneys at Law
1180 Avenue of the Americas
New York, New York 10036-8403
---
(212) 382-0700

Telex
23 6925

Facsimile
(212) 382-0888

Cable
Ostrofaber NewYork

jc555 U.S. PTO 04/15/99
jc549 U.S. PTO 09/292186 04/15/99

Express Mail #EM023991215US

Asst. Commissioner of Patents and Trademarks
Washington, DC 20231

OFGS File No. : IR-1609 (2-1941)
Inventor : Daniel M. Kinzer
Title : P-CHANNEL TRENCH MOSFET STRUCTURE
Assignee : International Rectifier Corporation

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

14 Pages of Specification including Abstract and Claims
8 Numbered Claims Calculated as 8 Claims for Fee Purposes
4 Sheets of Drawing Containing Figures 1 to 10. (Informal)
X Declaration and Power of Attorney
X Priority is Claimed under 35 U.S.C. §119:
Convention Date April 23, 1998 for United States Appln. S.N. 60/082,803
_____ Certified Priority Application
_____ Verified Statement Claiming Small Entity Status under 37 C.F.R. §1.27.
X Assignment
X Return-Addressed Post Card
OFGS Check No. 93848, which includes the fee of $800.00, calculated as follows:

Basic Filing Fee:	$ 760.00
Additional Filing Fees:	
Total Number of Claims in Excess of 20, times $18:	-0-
Number of Independent Claims in Excess of 3, times $78: . .	-0-
One or More Multiple Dependent Claims: Total $260.	-0-
Total Filing Fees or	$ 760.00
Total Filing Fee Reduced 50% for Small Entity:	-0-
Assignment Recording Fee: $40	40.00
TOTAL Filing Fee and Assignment Recording Fee:	$ 800.00

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed, or if any additional fee during the prosecution of this case is not paid, the Patent and Trademark Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

EXPRESS MAIL CERTIFICATE

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee (mail label #EM023991215US) in an envelope addressed to: Asst. Commissioner of Patents and Trademarks, Washington, D.C. 20231, on April 15, 1999
Dorothy Jenkins

Name of Person Mailing Correspondence

Dorothy Jenkins

Signature

April 15, 1999

Date of Signature

Respectfully submitted,

Samuel H. Weiner
Registration No.: 18,510
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

TRAN\300417

P-CHANNEL TRENCH MOSFET STRUCTURE

RELATED APPLICATIONS

This application is related to copending application Serial No. 08/299,533, filed September 1, 1994 entitled PROCESS FOR MANUFACTURE OF MOS GATED DEVICE WITH REDUCED MASK COUNT (IR-1113); and application Serial No. 60/104,148, filed October 14, 1998 entitled MOSGATED DEVICE WITH TRENCH STRUCTURE AND REMOTE CONTACT AND PROCESS FOR ITS MANUFACTURE (IR-1461).

BACKGROUND OF THE INVENTION

This invention relates to power MOSgated devices and more specifically relates to a novel low voltage P-channel MOSFET having a reduced switching loss.

Power Mosgated devices are well known and include such devices as power MOSFETs; IGBTs; gate controlled thyristors and the like. In low voltage applications of such devices, particularly in connection with battery operated portable electronic devices, such as personal computers, cellular telephones and the like, frequently termed wireless systems, careful power management is essential to extend the battery life and its usage between charges.

Power management applications in wireless systems fall generally into two categories. One category is charging the battery from an external DC source. it is important to control both the charging current and voltage correctly for the particular battery technology. This control is accomplished by modulating the duty cycle of a transistor placed between the power source and the battery in well known ways. The second category activates a portion of the system on demand. In this

case the transistor is placed between the battery and the load to be activated, such as an RF power amplifier. In some systems, multiple power supply voltages require DC/DC conversion as well. This may be accomplished with well known low dropout linear regulators or buck and boost switching regulators.

Both N-channel and P-channel power MOS transistors as the transistor in the above applications are available. P-channel devices are generally easier to use in these circuits. Thus, when the P-channel MOSFET is placed in the power bus, it can be controlled with a logic input that switches between the power rail and ground. This allows a single uninterrupted ground for the whole system. N-channel devices in the power bus require a gate signal that is boosted to a voltage higher than the bus, which requires extra circuitry.

In the past, the simplicity of a P-channel device came at the price of increased losses. This is because P-channel devices rely on hole conduction, and holes have a lower carrier mobility in silicon than electrons. The on-resistance of the active transistor is proportional to the carrier mobility, and its losses are proportional to the on-resistance, R_{DSON}.

To overcome this limitation, the length of the resistive path should be minimized and the width maximized within the transistor. The number of holes in the path must also be maximized. One way to do this is to lower the maximum voltage rating as much as possible which permits the use of lower resistivity and higher dopant concentration silicon.

Since most batteries operate at only a few volts, a 12V rating is generally more than enough for a transistor in a wireless application. Previously

available devices are rated at 20V, and have a reasonably low value of R_{DSON} at 2.5V gate to source. These parts come in various die sizes and package styles, ranging from the Micro 3 (SOT23) up to the SO8. The values listed in the following Table are for single transistors in a package, though the Micro 8 and SO8 packages also have dual versions. The power loss using these devices can be as high as 9% which translates directly into reduced usage.

Load Current	Part Number	Package Style	R_{DSON} @ 2.5V	V_{drop} or P_{diss} (as % of 5V supply)
500 mA	IRLML6302	*Micro 3™*	0.9 Ω	9%
1 A	IRLMS6702	*Micro 6™*	0.4 Ω	8%
2 A	IRF7604	*Micro 8™*	0.13 Ω	5%
4 A	IRF7416	SO-8	0.035 Ω	3%

It is known that a low voltage power MOSFET can be made with trench type technology to obtain reduced R_{DSON}, gate to drain capacitance, and to reduce Q_g (gate charge). Switching losses are proportional to the product of the device R_{DSON} and Q_g so it would be desirable to also reduce R_{DSON} in such devices. The present P-channel trench type power MOSFET uses a P-type substrate with a P-type epitaxial layer thereon. The device channel regions are formed by deep N-type diffusions from the top surface of the epitaxial layer, followed by P-type source diffusions. The voltage is then mostly blocked in the P-type epitaxial layer, resulting in a fairly large resistive drop, and in

increased losses in a wireless system. These losses in turn reduce battery life between charges.

BRIEF DESCRIPTION OF THE INVENTION

In accordance with the invention, in a P-channel trench type MOSgated device, the conventional P-type substrate epitaxial layer is eliminated and the diffused channel is replaced by an epitaxially grown N-type channel region. The channel region now has a uniform concentration, and the relatively lower doping of the channel region allows voltage to be blocked in the channel region and reduces the threshold voltage V_T for turn-on. Thus, with the novel structure, a major component of the on-resistance is removed and the device can be completely turned on at a gate to source voltage of 2.5 volts.

When the novel die of the invention is packaged in the same packages reported in the above Table, the R_{DSON} and power loss has been reduced up to 4 times, as shown in the following Table:

Load Current	Part Number	Package Style	R_{DSON} @ 2.5V	V_{drop} or P_{diss} (as % of 5V supply)
500 mA		*Micro 3™*	0.18 Ω	1.8%
1 A		*Micro 6™*	0.075 Ω	1.5%
2 A		*Micro 8™*	0.025 Ω	1%
4 A		SO-8	0.010 Ω	.8%

Thus, as shown above, overall circuit losses are reduced to less than 2% even at the discharged battery 2.5 volt condition.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of the junction pattern of a single cell of a prior art type of trench type P-channel MOSFET.

Figure 2 is a cross-section like that of Figure 1, but illustrates the junction pattern and structure of the present invention.

Figure 3 shows a circuit diagram of two MOSFETs like those of Figure 1 or 2, connected to form a bidirectionally conductive device.

Figure 4 is a cross-section similar to that of Figure 2, but shows a revised junction pattern by which a bidirectional MOSFET is formed.

Figure 5 is a circuit diagram of the bidirectional FET of Figure 4.

Figure 6 is a top view of a portion of the silicon substrate used to make the device of Figure 2.

Figures 7, 8, 9 and 10 show the appearance of the cross-section of the silicon of Figure 6, taken across section line 7-7 in Figure 6, following various process steps.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring first to Figure 1, there is shown one "cell" of a prior art P-channel trench type MOSFET. The single cell shown will be replicated any number of times over the surface of a chip.

Thus, the device has a P^+ doped substrate 20 which has an epitaxially deposited, lightly doped P^-

layer 21 thereon. An N^+ channel diffusion 22 is diffused into the upper surface of P^- layer 21 and is, therefore a graded diffusion. Trenches such as spaced trenches 23 and 24 are etched into the upper surface of the wafer or chip which is shown and extend below the bottom of channel diffusion 22. These trenches are lined with a gate insulation layer, such as an oxide, shown as gate oxide layers 25 and 26 in trenches 23 and 24 respectively and are filled with conductive polysilicon gates 28 and 29 respectively which are connected to one another (not shown) and to a common gate electrode. P^+ source diffusions 30, 31, 32 and 33 are formed at the top of trenches 23 and 24 respectively. Note that trenches 23 and 24 may be elongated stripe structures and that source regions 30 to 33 will also be elongated stripes. However, trenches 23 and 24 may also be polygonal in topology, in which case, the P^+ sources will surround restive trenches. Trenches may also surround the polygonal P^+ sources. Oxide insulation plugs 35 and 36 overlie polysilicon stripes 28 and 29 and insulate the polysilicon stripes from an overlying aluminum source contact 40. Source contact 40 contacts source regions 30, 31, 32 and 33 as well as the channel diffusion 22 in the usual manner. A drain contact 41 is connected to the bottom of the die to complete the vertical conduction trench device.

In operation, a sufficiently high gate voltage must be applied to polysilicon gates 28 and 29 to cause the graded channel diffusion 22 to invert along its entire length from sources 30 to 33 to the P^- epi layer 21. Thus, a relatively high gate voltage is needed to ensure inversion of the higher concentration portions of the channel diffusion. Further, once the device is

turned on, carriers flowing between drain 41 and source 40 see the relatively high resistance R_{epi} of layer 31, thus causing an increased R_{DSON} for the devices.

The present invention provides a novel structure which permits the use of a lower gate voltage and which has a lower R_{DSON} in a P-channel trench type MOSgated device. This device is shown in Figure 2 where components similar to those of Figure 1 have the same identifying numerals.

It will first be noted that the source contact in Figure 2 is made to P^+ source stripes 30, 31, 32 and 33 in the manner shown in copending application (IR-1113) Serial No. 08/299,533. Thus, a notch 50, for example, is etched through the P^+ source stripes to enable the source electrode 40 to contact the P^+ source stripes 31-33 and the underlying N-type channel regions. An N^{++} diffusion 51 may also underlie the bottom of the control notch to improve the contact between aluminum source 40 and silicon 60.

In accordance with the invention, the graded channel diffusion 22 and P^- epi layer 21 of Figure 1 are replaced by an N^+ epitaxially grown layer 60, grown directly on P^+ substrate 20. The N^+ layer 60 has a constant concentration along its full depth (a zero vertical gradient), and receives the various trench structures 23, and 24. Its concentration is selected to provide a low threshold voltage V_7. P^+ sources 30 to 33 are diffused into the top of N^+ epi layer 60.

As a result of the new structure, a reduced threshold voltage can be obtained, to allow about 2.5 volts to turn the device fully on, because the concentration along the full length of the invertible

layer adjacent the trench side walls is uniformly low. Further, the on resistance of the device is reduced because the resistance component R_{epi} in Figure 1 is removed from the device of Figure 2.

The device of Figures 1 or 2 can also be made as a bidirectional MOSFET as shown in Figure 4 for the device of Figure 2. Thus, the device of Figure 4 is identical to that of Figure 2 except that the source contact 40 contacts only the P^+ source regions 30-33, and does not contact channel region 60.

The structure of Figure 4 provides a single bidirectional MOSFET using less silicon area and having less on-resistance than that of two series connected MOSFETs such as those of Figures 1 and 2 to create a bidirectionally controlled circuit. Thus, in the past, two vertical conduction MOSFETs 70 and 71 must be connected in series between terminals 72 and 73, and will have a common gate terminal 74 to permit bidirectional control of circuit at terminals 72 and 73, as shown in Figure 3. By contrast, as shown in Figure 5, device 80, which is the device of Figure 4, will provide bidirectional control between terminals 72 and 73. However, the device and circuit of Figures 4 and 5 will have one-half of the R_{DSON} of the circuit of Figure 3, and will have one half of the silicon area.

Figures 6 through 10 describe a preferred process to manufacture the device of Figure 2. Similar numerals of Figures 1 and 2 describe similar elements in Figures 6 through 10.

The starting wafer for the process for a 12 volt P-channel device is a boron doped P^+ substrate 20 having a resistivity of less than 0.005 ohm cm and a thickness of 375 μm. An N^+ epitaxial layer 60 is grown

atop substrate 20 and is phosphorous doped with a resistivity of 0.17 ohm cm and a thickness of 2.5 μm.

The first major step, shown in Figures 6 and 7, is the formation of a trench mask atop the epitaxial layer 60, and the etching of trenches 23, 24 and others, to a depth of about 1200Å. The trench sidewalls are then prepared for gate oxidation and an initial sacrificial oxidation is carried out, leaving the device as shown in Figure 7.

Thereafter, and as shown in Figure 8, gate oxide layers 25 and 26 are grown inside the trench walls (and over the upper silicon surface). The gate oxide is grown for 30 minutes at 950°C 02/TCA.

Next, and as also shown in Figure 8, polysilicon is grown over the upper surface of the wafer and into the trenches as polysilicon gates 28 and 29. The polysilicon is grown to a thickness of about 7,500Å. After the polysilicon is grown, it is made conductive by a boron implant with a dose of 1E14 and an energy of 80 KeV. This implant is followed by an anneal and drive step at 1050°C for 60 minutes in nitrogen. A mask is then applied to etch the polysilicon off the top of the active device surface (the termination is not described herein and is conventional) and the wafer then appears as shown in Figure 8.

Thereafter, there is a polyoxidation step at 975°C for 40 minutes at 02/TCA to grow oxide atop the poly in each trench. The source implant step is then carried out to form the P^+ implants shown in Figure 9, which will become the P^+ source regions 30 to 33 of Figure 2. The source implant in Figure 9 is a boron implant at a dose of 2E15 and an energy of 50 KeV. Next,

as shown in Figure 9, a TEOS insulation layer 35, 36 is deposited atop the wafer to a thickness of 7,500Å.

Next, and as shown in Figure 10, a source drive is carried out to drive the P^+ source regions into the silicon, driving at 850°C for 30 minutes in nitrogen.

The final steps applied to the wafer of Figure 10 produce the structure shown in Figure 2, and include a contact mask step to open the contact windows, followed by the formation of N^{++} layer 51 to improve the contact between the silicon and the aluminum source metal. The region 51 may be formed by a phosphorous implant with a dose of 1E15 and energy of 50 KeV. After suitable metal deposition preparation, aluminum front metal 40 is applied by sputtering to a thickness of 8 μm.

Thereafter, the wafer 20 is reduced in thickness to 210 μm as by grinding, and the back metal or drain 41 is suitably deposited, forming the device as shown in Figure 2.

In carrying out the above process, a trench width of 0.6 μm and a mesa width of 1.8 μm have been used. Other dimensions can be selected. Further, a square cell has been used, although a stripe can be used. After completion of the wafer, die have been formed with dimensions of 75 mils x 90 mils with 88% being active area. Larger die sizes of 102 mils (2.591 mm) x 157 mils (3.988 mm) with 92% being active area, have also been used.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be

limited not by the specific disclosure herein, but only by the appended claims.

Exhibit 1003 - Page 20 of 20

WHAT IS CLAIMED IS:

1. A trench-type power MOSFET having a vertical invertible channel of one of the conductively types disposed between a source region and a drain region; a gate oxide and gate contact thereon extending along the length of said invertible channel and operable to invert the conductivity type of said invertible channel; said vertical invertible channel having a constant concentration along its full length.

2. The power MOSFET of claim 1 wherein said one of the conductivity types is the N-type.

3. The power MOSFET of claim 1 wherein said invertible channel is epitaxially deposited silicon.

4. A power MOSFET comprising, in combination; a substrate of one of the conductivity types; an epitaxially deposited layer of the other conductivity type deposited atop said substrate and having a substantially constant concentration; a plurality of spaced trenches having vertical walls extending through said epitaxial layer; a thin gate oxide on said vertical walls and conductive polysilicon deposited into said trenches to define a polysilicon gate; a source region of said one conductivity type formed adjacent the walls of each of said trenches and diffused into the top of said epitaxial layer; a source contact connected to at least said source regions; a drain contact connected to said substrate; whereby said MOSFET has a reduced on resistance.

5. The MOSFET of claim 4 wherein said source contact is connected to said source region only, whereby said MOSFET is bidirectional.

6. The MOSFET of claim 4 wherein said source contact is connected to said epitaxially deposited layer.

7. The MOSFET of claim 4 wherein said one conductivity type is the P-type.

8. The MOSFET of claim 7 wherein said epitaxial region has a resistivity of about 0.17 ohm cm and a thickness of about 2.5 μm.

IR-1609 (2-1941)

P-CHANNEL TRENCH MOSFET STRUCTURE

ABSTRACT OF THE DISCLOSURE

A low voltage P-channel power MOSFET using trench technology has an epitaxially deposited constant concentration N channel region adjacent the side walls of a plurality of trenches. The constant concentration channel region is deposited atop a P^+ substrate and receives P^+ source regions at the tops of each trench. The source contact is connected to both source and channel regions for a unidirectional conduction device, or only to the source regions for a bidirectional device.

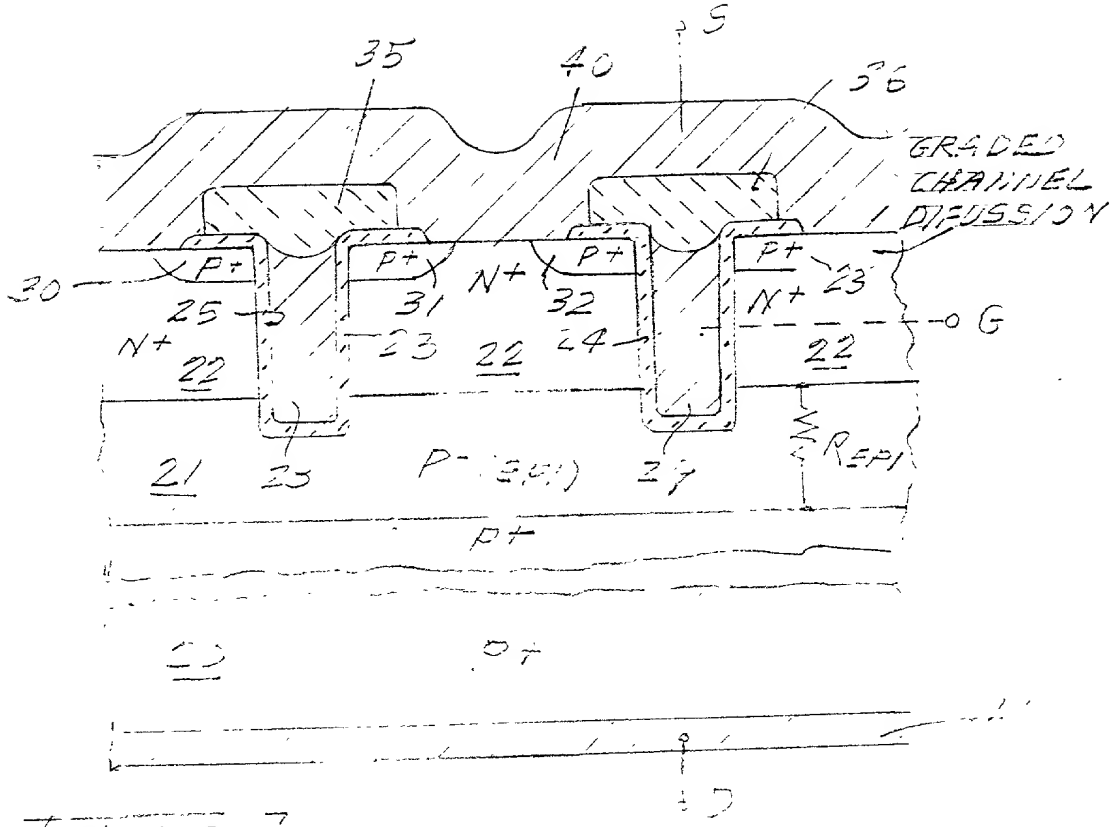

FIG. 1
(PRIOR ART)

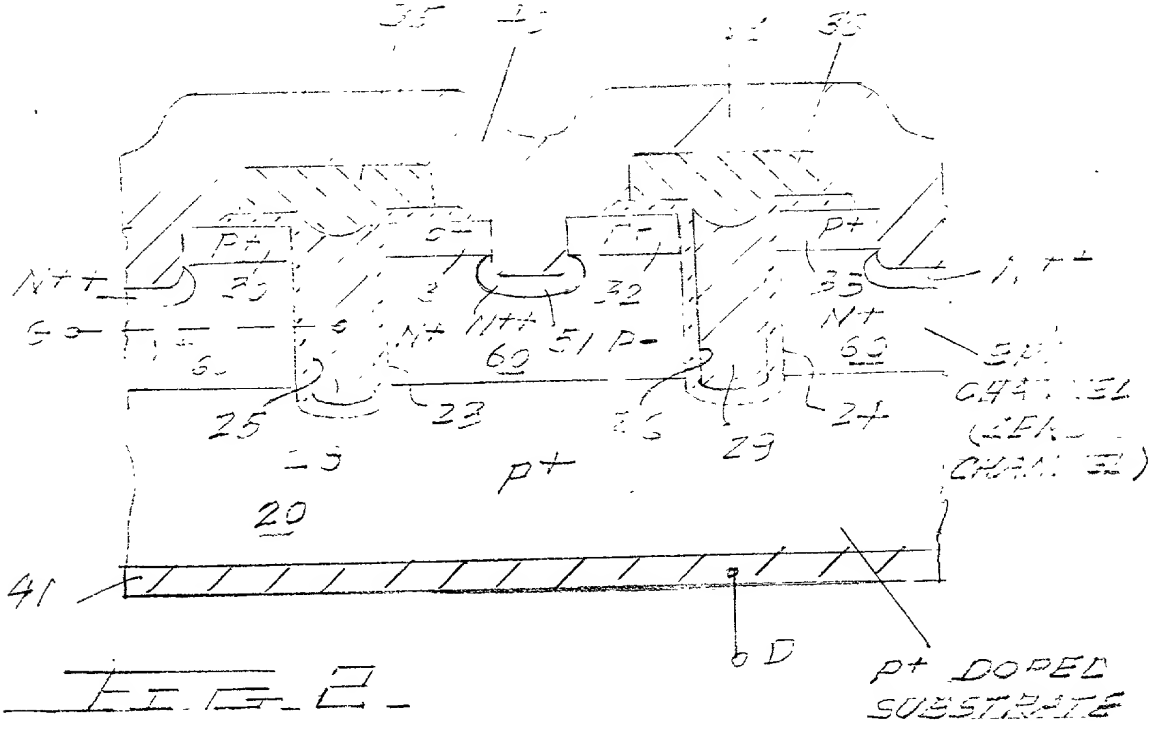

FIG. 2

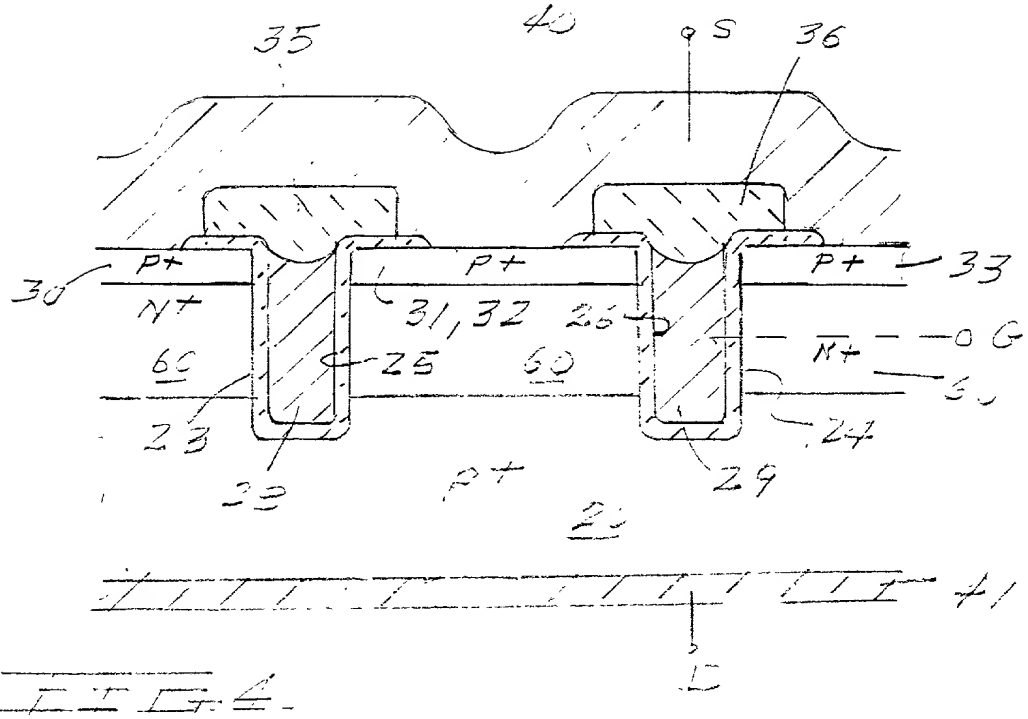

FIG. 4.

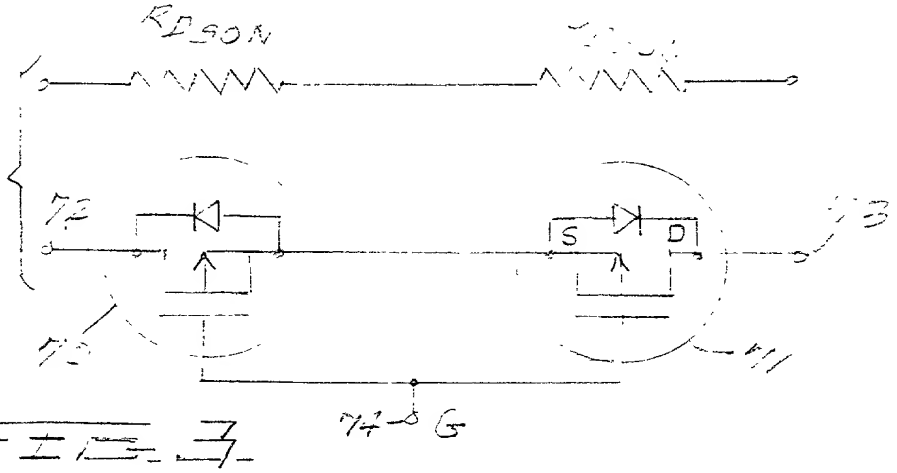

FIG. 3.

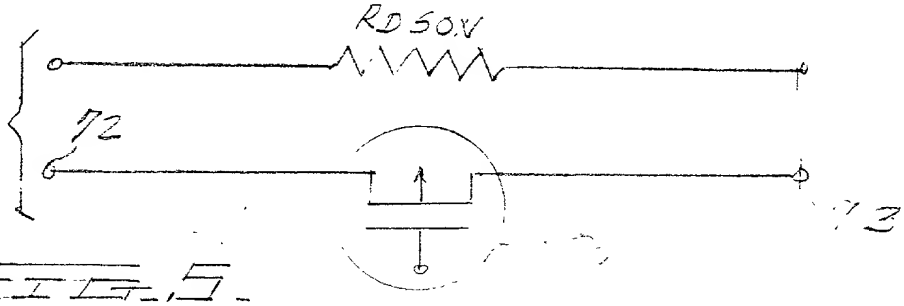

FIG. 5.

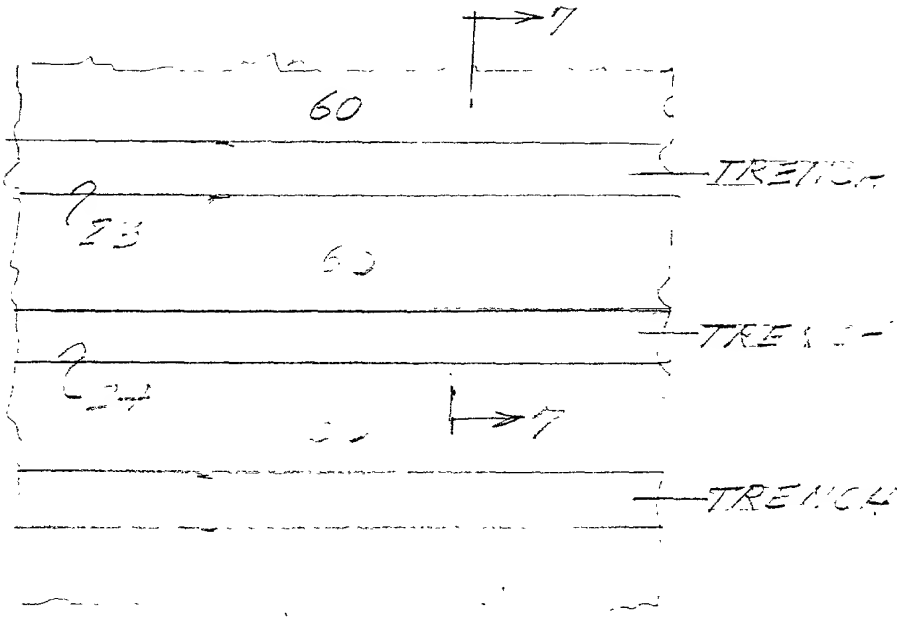
7
60
TRENCH
23
50
TRENCH
24
7
TRENCH

FIG. E.

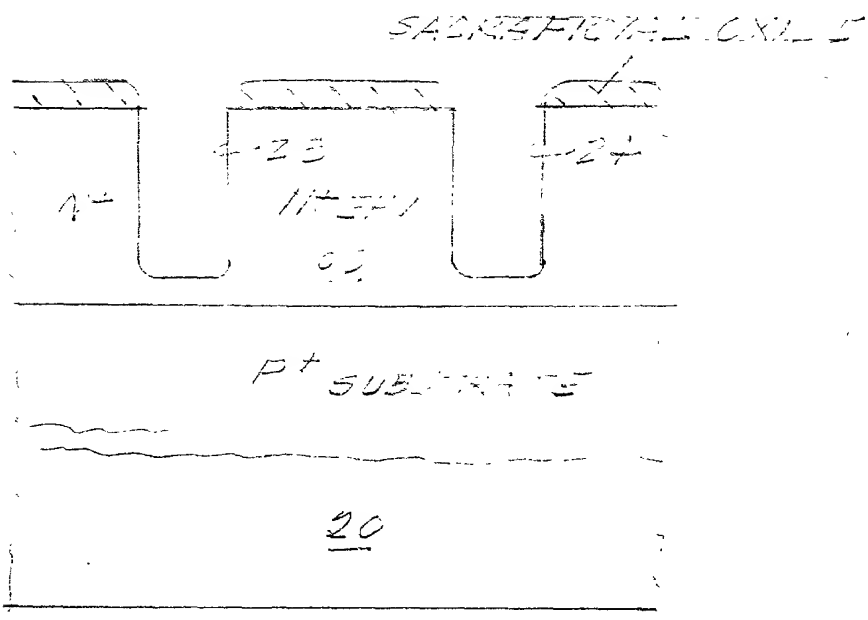
SACRIFICIAL OXIDE
23
24
P+ SUBSTRATE
20

FIG. 7

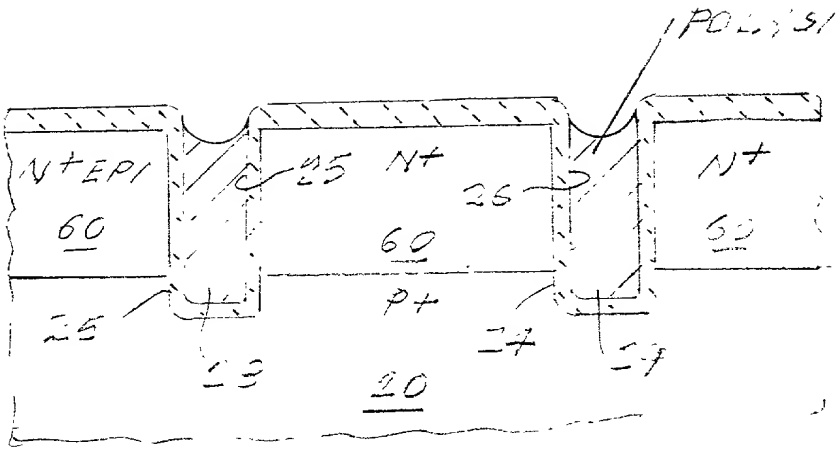

FIG. 8

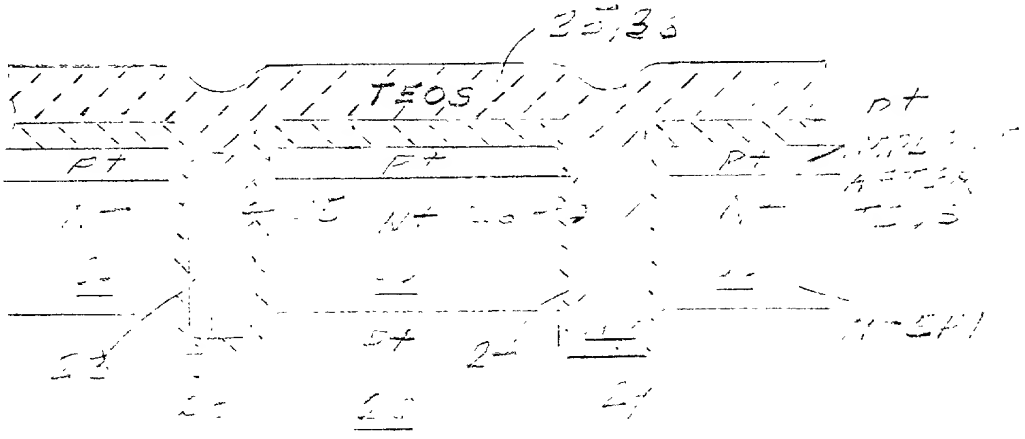

FIG. 9

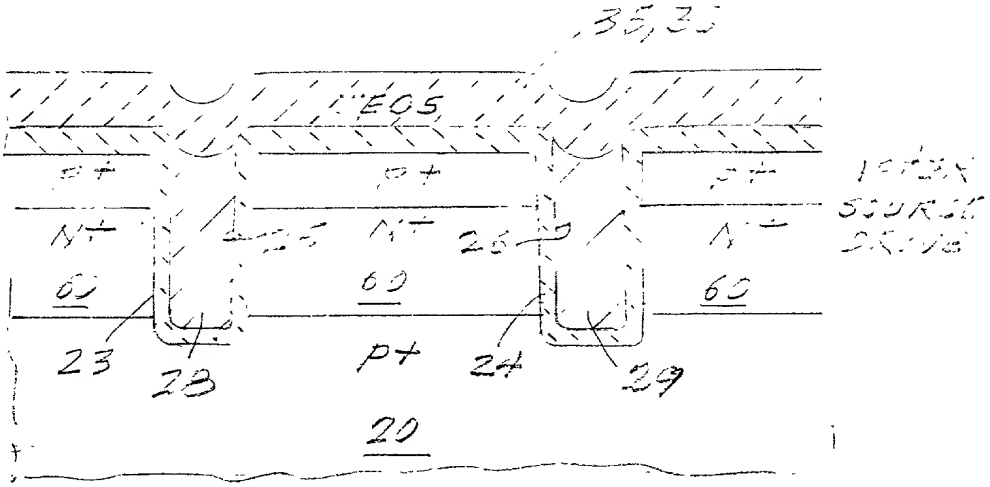

FIG. 10

UNITED STATES OF AMERICA COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION	OFGS FILE NO. IR-1609 (2-1941)

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

P-CHANNEL TRENCH MOSFET STRUCTURE

the specification of which is attached hereto, unless the following box is checked:

☐ was filed on _____ as United States patent Application Number or PCT International patent application number _____ and was amended on _____ (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign or Provisional Application(s)

COUNTRY	APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	PRIORITY CLAIMED UNDER 35 U.S.C. 119
U.S.A.	60/082,803	April 23, 1998	YES X NO ___
			YES ___ NO ___
			YES ___ NO ___

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

UNITED STATES APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	STATUS *(patented, pending, abandoned)*

I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB & SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944; Louis C. Dujmich - Reg. No. 30,625 and Douglas A. Miro - Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.

SEND CORRESPONDENCE TO: **OSTROLENK, FABER, GERB & SOFFEN, LLP**
1180 AVENUE OF THE AMERICAS
NEW YORK, NEW YORK 10036-8403
CUSTOMER NO. 2352

DIRECT TELEPHONE CALLS TO:
(212) 382-0700

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	INVENTOR'S SIGNATURE	DATE
Daniel M. Kinzer	Daniel M Kinzer	4/14/99
RESIDENCE *(City and either State or Foreign Country)* El Segundo, California 90245		COUNTRY OF CITIZENSHIP United States
POST OFFICE ADDRESS 760 Center Street El Segundo, California 90245		
FULL NAME OF SECOND JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE
RESIDENCE *(City and either State or Foreign Country)*		COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS		
FULL NAME OF THIRD JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE
RESIDENCE *(City and either State or Foreign Country)*		COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS		